

**UE/HE910V2\_DE/CE910\_HE920\_CL865**  
**Digital Voice Interface**  
**Application Note**

80000NT10101A Rev.1 2015-06-19



## APPLICABILITY TABLE

PRODUCT
DE910-xxx
HE910-xxx V2
CE910-xxx
UE910-xxx V2
HE920-xxx
CL865-xxx



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# 1 Introduction

## 1.1 Scope

The aim of this document is the description of some hardware specification useful to develop a product using Telit modules supporting DVI (PCM), as specified in the aforementioned applicability table.

## 1.2 Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our UE/HE910V2\_DE/CE910\_HE920\_CL865 modules.

## 1.3 Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit's Technical Support Center (TTSC) at:

[TS-EMEA@telit.com](mailto:TS-EMEA@telit.com)  
[TS-NORTHAMERICA@telit.com](mailto:TS-NORTHAMERICA@telit.com)  
[TS-LATINAMERICA@telit.com](mailto:TS-LATINAMERICA@telit.com)  
[TS-APAC@telit.com](mailto:TS-APAC@telit.com)

Alternatively, use:

<http://www.telit.com/en/products/technical-support-center/contact.php>

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

<http://www.telit.com>

To register for product news and announcements or for product questions contact Telit's Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.



## 1.4 Document Organization

This document contains the following chapters:

Chapter 1: “Introduction” provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: “Overview” provides an overview of the document.

Chapter 3: “UE/HE910V2\_DE/CE910\_HE920\_CL865 DVI” describes the DVI port as far as the UE/HE910V2\_DE/CE910\_HE920\_CL865 modules are concerned

Chapter 4: “Protocol description”

Chapter 5: “Parameters and timing characteristics”

Chapter 6: “Custom AT commands”

Chapter 7: “External codec” provides an example of interfacing with an external audio codec.

## 1.5 Text Conventions



***Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.***



***Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.***



**Tip or Information – Provides advice and suggestions that may be useful when integrating the module.**

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.



## 1.6 Related Documents

- Software User guide
- Hardware User Guide
- Product description
- AT Commands Reference Guide

## 1.7 Document History

Revision	Date	Changes
0	2013-06-25	First release
1	2015-06-19	Fixed figure 3 Deleted figure 4 Added CL865 Changed External Codec to MAX9867



## 2 Overview

The Telit Modules support the **Digital Voice Interface** (from here onwards **DVI**), which can be used to transfer digital audio data *to* and *from* the module itself.

The **DVI** uses the **PCM interface** as part of the audio front end; it easily allows for an external codec to be used instead of the internal codec.

As an example, through the **DVI** you could connect a Telit Module to a Bluetooth device.

### 2.1 Hint on PCM

Although analog communication is ideal for human communication, analog transmission is neither robust nor efficient at recovering from line noise.

As example in the early telephony network, when analog transmission was passed through amplifiers to boost the signal, not only was the voice boosted but the line noise was amplified, as well. This line noise resulted in an often-unusable connection.

It is much easier for digital samples, which are comprised of 1 and 0 bits, in order to be separated from line noise. Therefore, when analog signals are regenerated as digital samples, a clean sound is maintained.

PCM converts analog sounds into digital form by sampling the analog sounds 8000 times per second and converting each sample into a numeric code. If you sample an analog signal at twice the rate of the highest frequency of interest, you can accurately reconstruct that signal back into its analog form (Nyquist theorem). Because most speech content is below 4000Hz, a sampling rate of 8000 times per second (8KHz that means 125  $\mu$ Sec between samples) is required.

### 2.2 General information

The Telit Modules can have one **DVI** port.

Please refer to the User Guide of the module that you are using to know the number of the available **DVI** port.











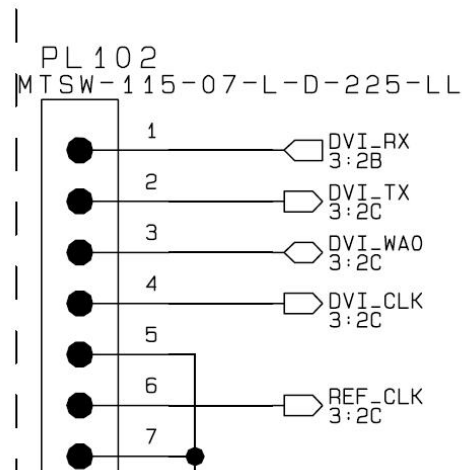


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**Figure 3.2 DVI Pin displacement on CS1467x for xE910-xxx**

DVI Function	PL102
DVI_CLK	4
DVI_WA0	3
DVI_RX	1
DVI_TX	2

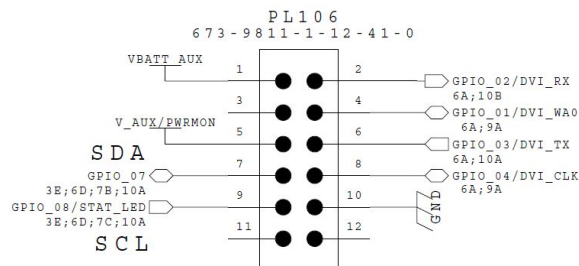
**Table 3.4 DVI signals Pin assignment on KS0145x for xE920-xxx**



**Figure 3.3 DVI Pin displacement on KS0145x for xE920-xxx**

DVI Function	PL106
GPIO_04/DVI_CLK	8
GPIO_01/DVI_WA0	4
GPIO_02/DVI_RX	2
GPIO_03/DVI_TX	6

**Table 3.6 DVI signals Pin assignment on CS1531x for CL865-xxx**



**Figure 3.5 DVI Pin displacement on CS1531x for CL865-xxx**





## 4 Protocol Description

The *DVI* operates in 16-bit data burst mode, starting with the most significant bit.

GSM voice is 13-bit 2's complement but the output of the speech decoder is saved on 16-bit 2's complement (Q15 format). The last 3 LSBs are equal to 0.

The frame lasts for 17 clock pulses, as one more clock pulse is needed for the frame synchronization of the signal *PCM\_SYNC*.

Following the falling edge of the *PCM\_SYNC* signal, the data bits are sampled at the module data input (RX) and module output data (TX) at the next falling clock (CLK) pulse edge.

All data is 8 kHz and 16 bits with DVI (PCM interface).

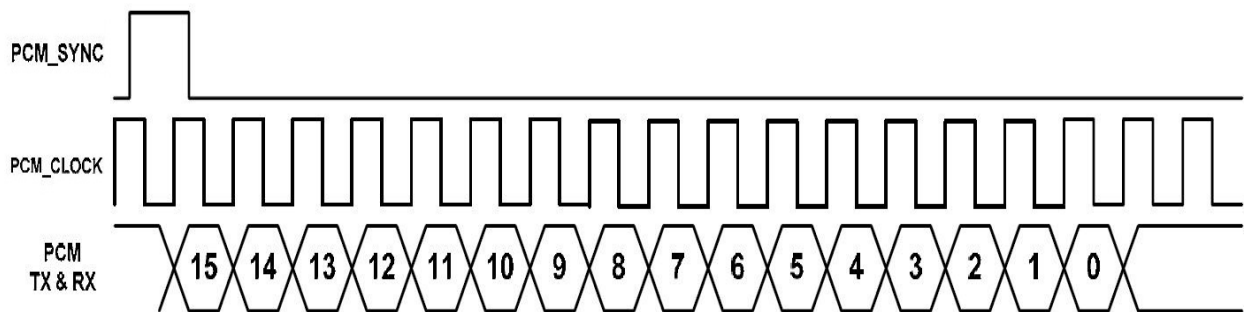


Figure 4.1 Digital Voice Interface (PCM) signal timing

### 4.1 Primary Mode

On *Primary* mode UE/HE910V2\_DE/CE910\_HE920\_CL865 provide a 16-bit linear or 8-bit A-law or  $\mu$ -law with padding, with short-sync and 2.048MHz clock (on the *PCM\_CLOCK* pin).

Both *Master* and *Slave* mode are allowed.



## 4.2 Auxiliary Mode

On *Auxiliary mode* UE/HE910V2\_DE/CE910\_HE920\_CL865 provide 16-bit linear or 8-bit A-law or  $\mu$ -law with padding, with *long-sync* and 128 KHz clock (on the **PCM\_CLOCK** pin).

Only *Master* mode is allowed.



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**NOTE:**

**UE910-xxx DOES NOT support Auxiliary Mode (128K / Long-sync).**

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## 5.2 Auxiliary PCM Interface

Parameter	Description	Min	Typical	Max	Units
t(auxsync)	PCM_SYNC cycle time		125		us
t(auxsynch)	PCM_SYNC high time	62.4	62.5		us
t(auxsyncl)	PCM_SYNC low time	62.4	62.5		us
t(auxclk)	PCM_CLOCK cycle time		7.8		us
t(auxclkh)	PCM_CLOCK high time	3.8	3.9		us
t(auxclk)	PCM_CLOCK low time	3.8	3.9		us
t(suauxsync)	PCM_SYNC setup time high before falling edge of PCM_CLOCK	1.95			us
t(hauxsync)	PCM_SYNC hold time after falling edge of PCM_CLOCK	1.95			us
t(suauxdin)	PCM_RX setup time before falling edge of AUX_PCM_CLK	70			ns
t(hauxdin)	PCM_RX hold time after falling edge of AUX_PCM_CLK	20			ns
t(pauxdout)	Delay from AUX_PCM_CLK rising to AUX_PCM_TX valid			50	ns

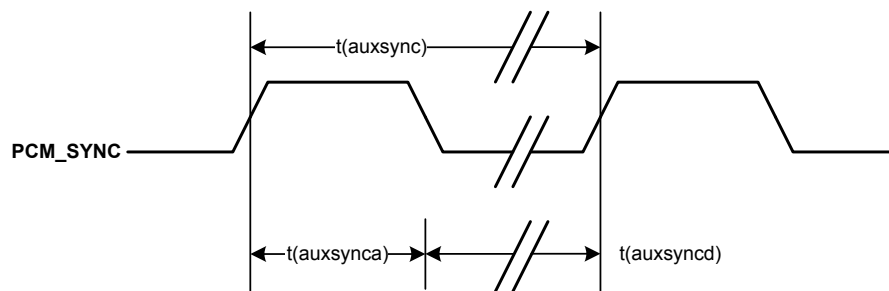


Figure 5.4 AUX PCM\_SYNC timing (only Long sync)

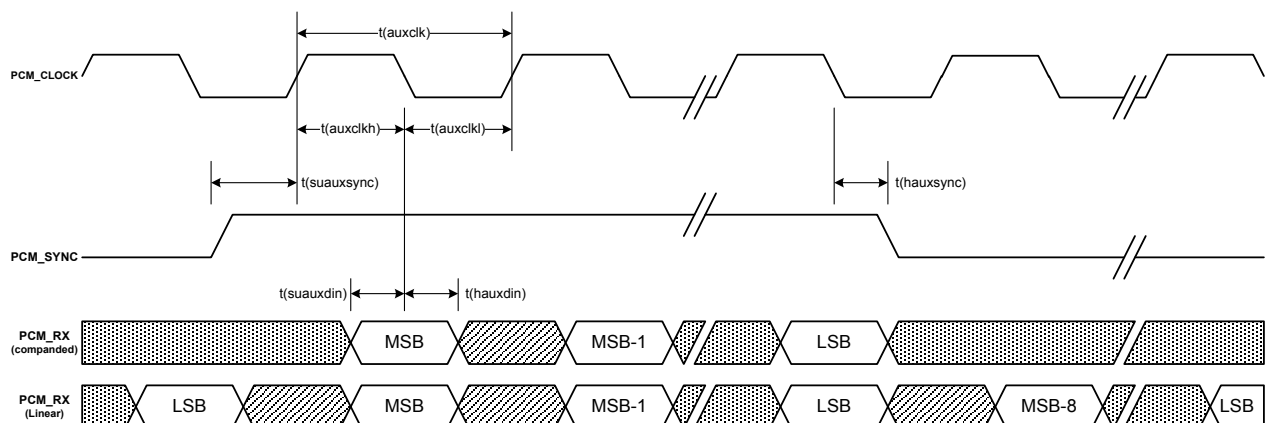


Figure 5.5 AUX External codec to UE/HE910V2\_DE/CE910\_HE920\_CL865 timing











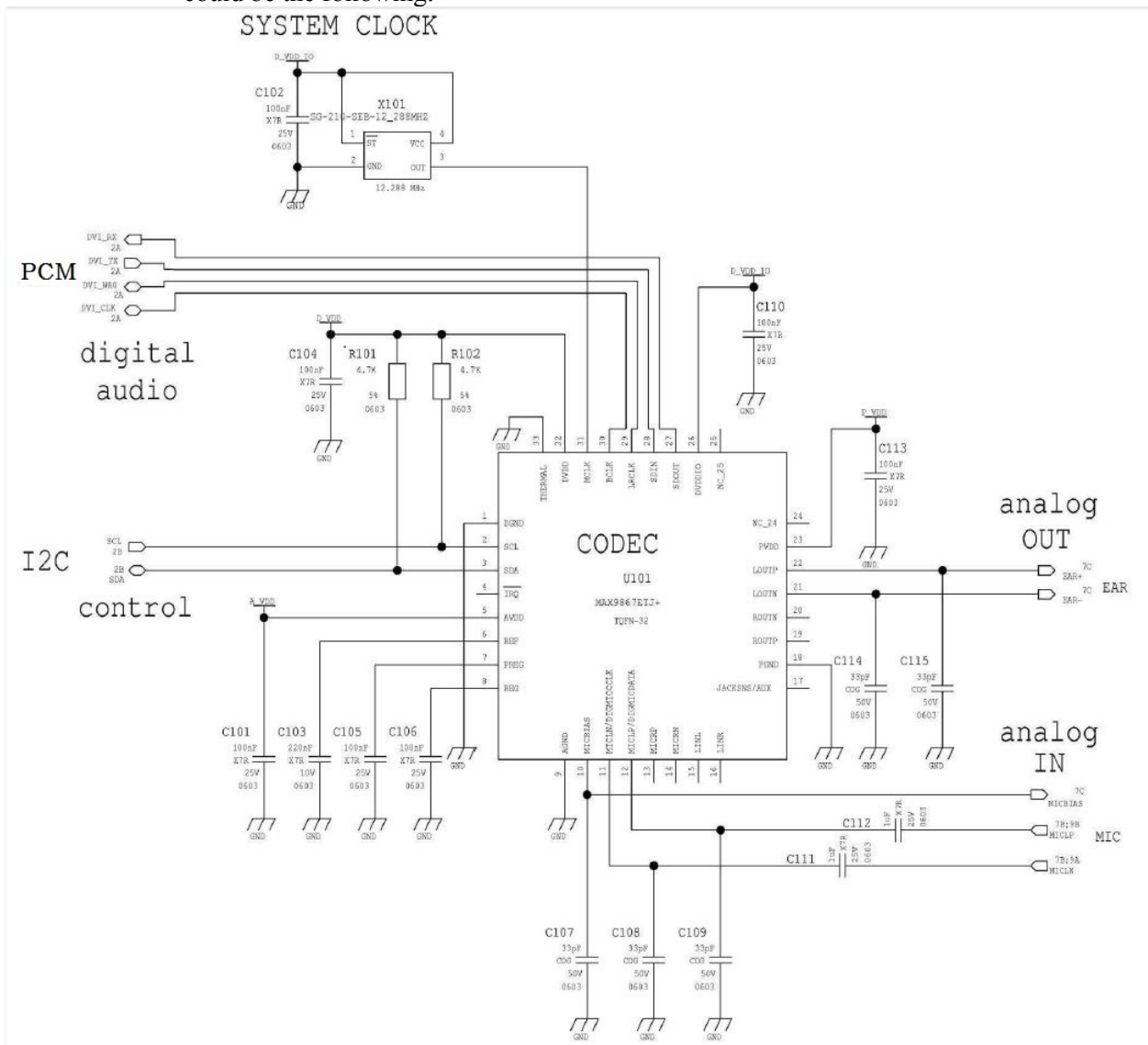
## 7 External Codec

The market offers great variety of audio codecs and, obviously, the customers will choose by itself the device that better fits their application.

Just as an example, in the following we go describing a possible interfacing with an external audio codec.

### 7.1 Schematic

A schematic example of an interface between the Telit's modules and the MAX9867 CODEC could be the following:





## 7.2 Codec and DVI settings

Speaker and microphone are connected to the external output input lines of the codec. MAX9867 is configured by a script file, sent by a modem like Procomm® or Hyperlink®. Every block defines some parameters to load:

- amplifiers gain
- signal mixing
- operating mode
- any other information needed

### 7.2.1 First step DVI signals routing

The DVI useful signals are routed to the assigned pin of the module. Refer to the Telit module's HW User Guide for all information on the used DVI signals.

- DVI\_TX, DVI\_RX, DVI\_WA0 and DVI\_CLK

### 7.2.2 Second step DVI configuration

- Clock rate =2.048 MHz
- PCM decoder padding on
- decoder linear
- PCM encoder padding on
- Encoder linear

*at command "AT#DVICFG=1,1,2,1,2"*

### 7.2.3 Last step DVI Activation and clock mode setting

- Enable DVI: audio is forwarded to the DVI block
- DVI port 4 will be used
- Clock mode DVI master

*at command "AT#DVI=1,2,1^M"*

